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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,703	08/05/2003	David B. Glasco	NWISP036	8389

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EXAMINER

THOMAS, SHANE M

ART UNIT	PAPER NUMBER
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2186

DATE MAILED: 07/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/635,703

Applicant(s)

GLASCO, DAVID B.

Examiner

Shane M. Thomas

Art Unit

2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 May 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office action is responsive to the response filed 5/17/2006. Claims 1-20 remain pending.

All previously outstanding objections and rejections to the Applicant's disclosure and claims not contained in this Action have been respectfully withdrawn by the Examiner hereto.

Excerpts from all prior art references cited in this Office action shall use the shorthand notation of [column # / lines A-B] to denote the location of a specific citation. For example, a citation present on column 2, lines 1-6, of a reference shall herein be denoted as "[2/1-6]."

Response to Arguments

Applicant's arguments with respect to claims 1-20 (pages 4-6 of the response) have been considered and are persuasive; the Examiner agrees that Hum does not make a specific reference to the plurality of processors being connected in a clear-cut point-to-point manner. For this reason, the Examiner has reviewed the previous prior art searched and has found a few references that teach Applicant's claims. As such, this Office action has been made Non-Final to give Applicant's a chance to respond to the new references and rejections.

Claim Objections

Claims 5,8,9,15,18, and 19, are objected to because of the following informalities:

As per claims 5,8,15, and 18, the Examiner recommends amending the term --the response-- to --the response information-- as the former term has not been previously defined in the claims.

Claims 9 and 19 are objected to as being dependent open objected to claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keller et al. (U.S. Patent No. 6,490,661) in view of Hughes (U.S. Patent No. 6,973,543).

As per claims 1,11, and 20, Keller teaches a **method** (figures 9 and 15) **for providing a response to a cache access request** (in this case a read request) **comprising:**

(1) receiving a cache access request (read command) **associated with a memory line** (line of memory requested to be read) **at a cache coherence controller** (memory controller 16 of figure 1 - [2/35-37]) **from a processor** (source processor 70 - figure 9) **in a cluster of**

Art Unit: 2186

processors (cluster of processors 12A-12D shown in figure 1), **the cluster of processors interconnected in a point-to-point architecture** (as taught in figure 1 and [2/28-30]);

(2) obtaining response information (read response - figure 9 - [13/1-3]) **for the cache access request from a remote data cache** (memory 421 [5/56-59] is associated with Target processor 72 is remote from the source processor 70 as it exclusively coupled to the target processor 72) **associated with the cache coherence controller** (controller 16 of target processor), **wherein the remote data cache 421 receives data [13/1-3] and state information** (figure 10B and [15/19-22]) **for the memory lines of remote clusters**. The Examiner is considering a **remote clusters** to be the hard drives (which comprise the entire address space of the system of figure 1) connected to the processing cluster (figure 1) by way of the I/O Bridge 20. Keller does not specifically state that hard drive(s) can be connected to the I/O bridge 20. Hughes teaches in figure 1 an almost identical multi-processor system configuration as Keller teaches in figure 1. Hughes teaches in [4/58-62] that hard drives may be connected to the processing system of figure 1 of Hughes by way of the I/O bridge 20A. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the multi-processor cluster system of Keller with the teaching of hard drive connections to a processing cluster by means of an I/O bus in order to have maintained a non-volatile storage encompassing the entire address space of the cluster system of figure 1 of Keller. Such a consideration by the Examiner to refer to the hard drives of modified Keller to be remote clusters is substantiated by Keller in that each processor node 12 of figure 1 only comprises a portion of the total address space of the system of Keller [5/47-53] and that the hard drives would be --remote-- from the processing cluster 12A-12D as the hard drives would be accessed

Art Unit: 2186

via the I/O bridge 20. Because each particular processing node would only own that particular portion of the total address space, it could therefore be seen that that particular processing node would have stored the respective **memory lines** of the total system address space (contained in whole on the hard drives as known in the art). The claim limitation does not specifically state that the remote clusters comprise other processing nodes (connected in a point-to-point fashion) and therefore may be broadly interpreted to comprise a hard drive cluster connected via an I/O bridge as discussed.

(3) determining that the cache access request can be handled locally (i.e. within the processing nodes 12A-12D) **by using the remote data cache** (memory 421 of target processor 72) **without having to probe remote nodes** (i.e. the hard drives of modified Keller). A read response, including the requested data, may be forwarded back to the source processor 70 from the target processor 72 - [13/1-3].

(4) providing response information (read response - [13/1-3]) **with a completion indicator to the processor when it is determined that the cache access request can be handled locally**. Keller does not specifically teach a completion indicator being sent with the read response; however, Hughes teaches such a completion indicator (NP bit - [13/60-63]) that can be included with the read response. It would have been further obvious to one having ordinary skill in the art at the time the invention was made to have combined the multi-processor cluster system of Keller with the teachings of Hughes in order to have utilized the completion indicator NP to inform the source (requesting) processor 70 that probe responses from the other processors 74 and 76 would not be required so that the source processor 70 may immediately use the requested data without waiting [11/55-59].

Art Unit: 2186

Claims 11 and 20, while not identical to claim 1, contain many similar or identical limitations and are therefore rejected for the same reasons as discussed directly above.

As per claim 2, **the cache access request can be handled locally if a valid copy of the memory line is in the remote data cache 421** - [2/66-3/3].

As per claims 3 and 13, **response information includes state information** (figure 10A - bits [7:6] of line 3 of the packet - and figure 10B) - [12/66-13/20].

As per claim 4, **the completion indicator is a completion bit (NP bit)** as taught by Hughes - [13/50-67].

As per claims 5 and 15, **the completion indicator notifies the processor 70 that the response from the cache coherence controller** (of target processor 72) **will be the only response** - [13/60-63] of Hughes. Hughes teaches here that if the completion response bit - NP - is activated, then no other response probes will be received from the other processors (74,76) in the cluster, and therefore will be the only response.

As per claim 6 and 16, **the processor 70 is a request processor** (as it may request data from a target processor 72 - figure 9) **in a request cluster** (figure 1). The Examiner is considering the cluster of processors 12A-12D to be a --request cluster-- when one of the processors is requesting data from another processor (via a remote data cache) within the cluster. For example, during the read request method of figure 9, the cluster can be considered to be a request cluster.

As per claims 7 and 17, **the completion indicator allows the cache coherence controller to avoid probing local [nodes]** (local nodes 74 and 76 - figure 9 of Keller - are not

Art Unit: 2186

probed if the completion bit NP is active as taught in Hughes - [13/60-63]) **or remote nodes** (hard drives connected to the processing cluster of figure 1 via I/O bridge).

As per claims 8 and 18, **the processor 70 sends a source done upon identifying the completion indicator in the response** (figure 9 of Keller and [11/49-55]).

As per claims 9 and 19, **the processor 70 sends the source done to the cache coherence controller** (of target processor 72 - [11/49-55]).

As per claim 10, **the processor 70 sends the source done to the cache coherence controller acting as a memory controller** (since the cache controller 16 is in fact a memory controller - [11/49-55]).

As per claim 12, **response information is provided in a response packet** as taught by Keller in [2/28-32], [3/66-67] and figure 5.

As per claim 14, **response information includes data** - [13/1-3] of Keller.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pentkovski et al. teaches a cluster of processors interconnected in a point to point manner and a remote data cache 420 in figure 4.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M. Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

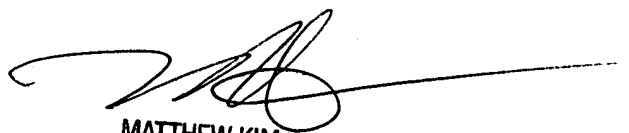
Art Unit: 2186

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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